California State University, Fullerton

Computer Engineering

**EGCP 446 – Advanced Digital Design using Verilog HDL**

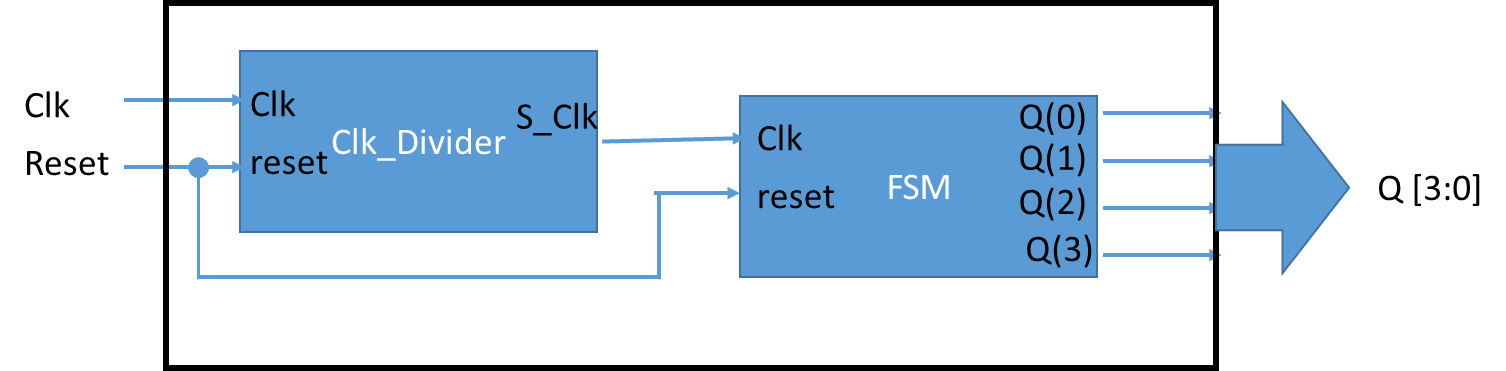
**(Fall 2019)**

**Lab No 4: ASM**

1. **Lab Description**

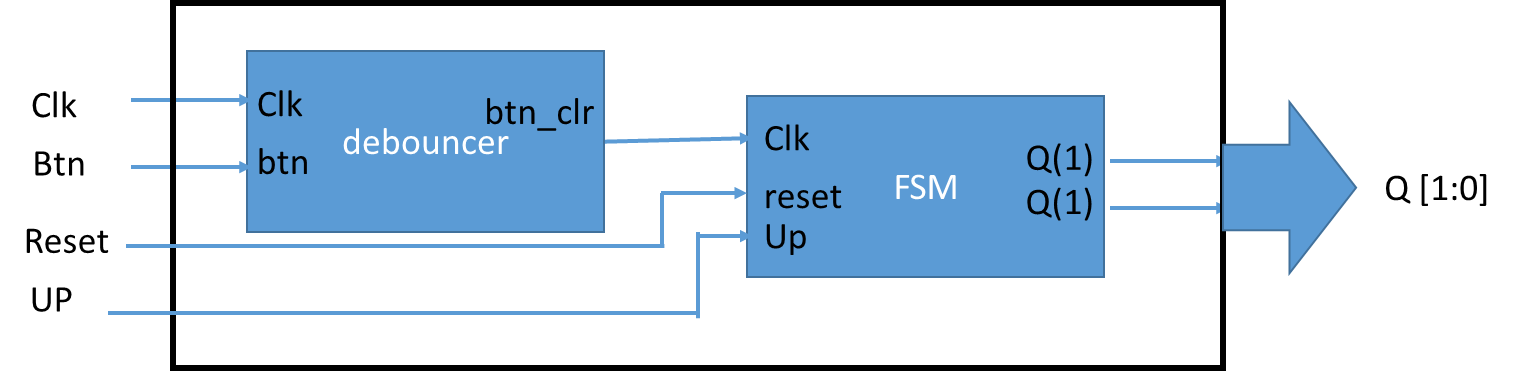
**Part A: Clock Divider**

Implement the lab no 3 part 1 on an FPGA board. Create a clock divider circuit to slow the clock from 50 MHz to 1 Hz. Connect the Clk with the system clock, Reset with the switch, and Q with the LED.



**Part B: Debouncer Circuit**

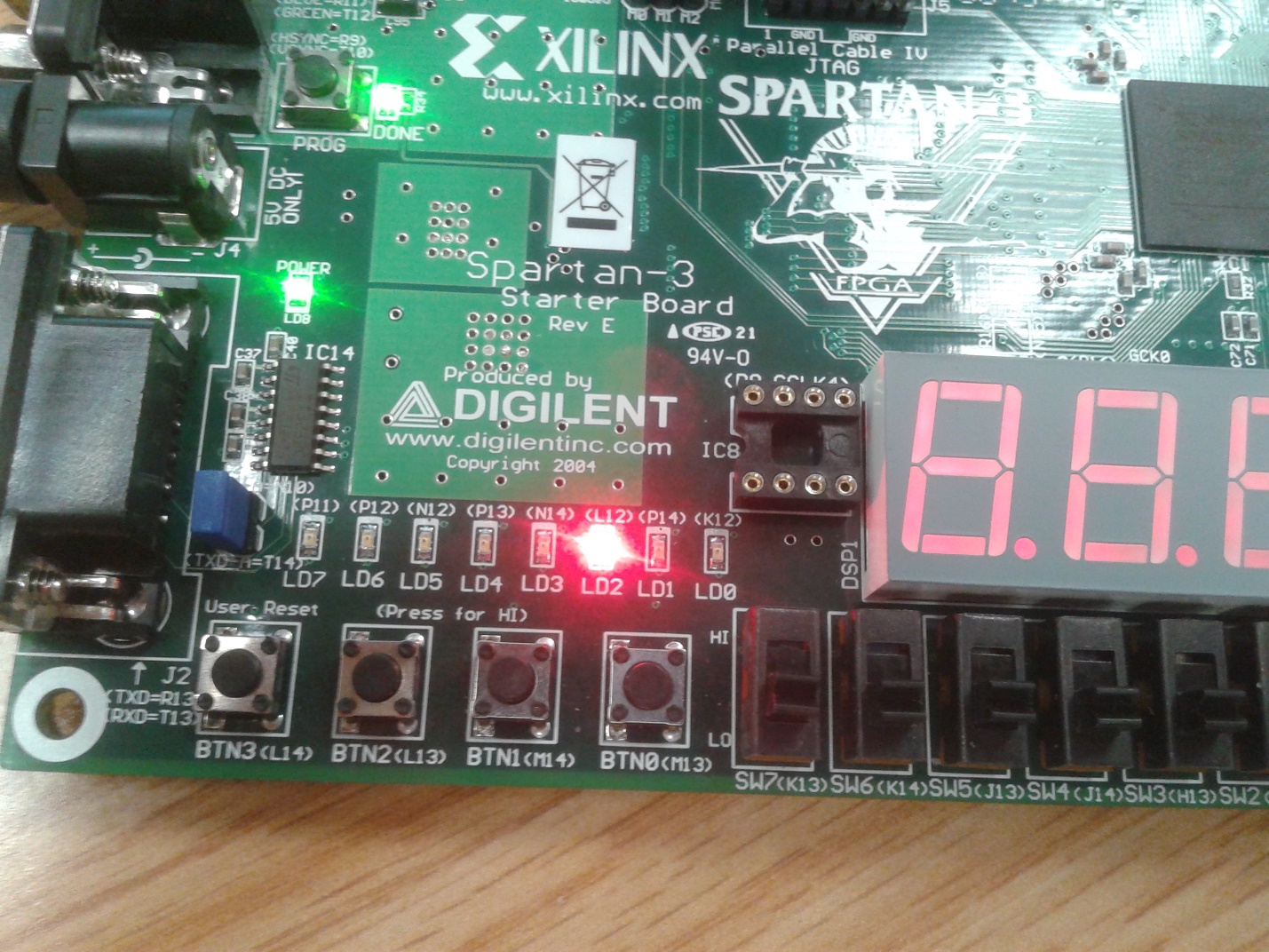
Implement the lab no 3 part 2 on an FPGA board. Instead of using a system clock, now use the debouncer Verilog code provided with the lab. Connect the clk of debouncer with system clock, btn with push-button, reset with switch, and Q with LED.

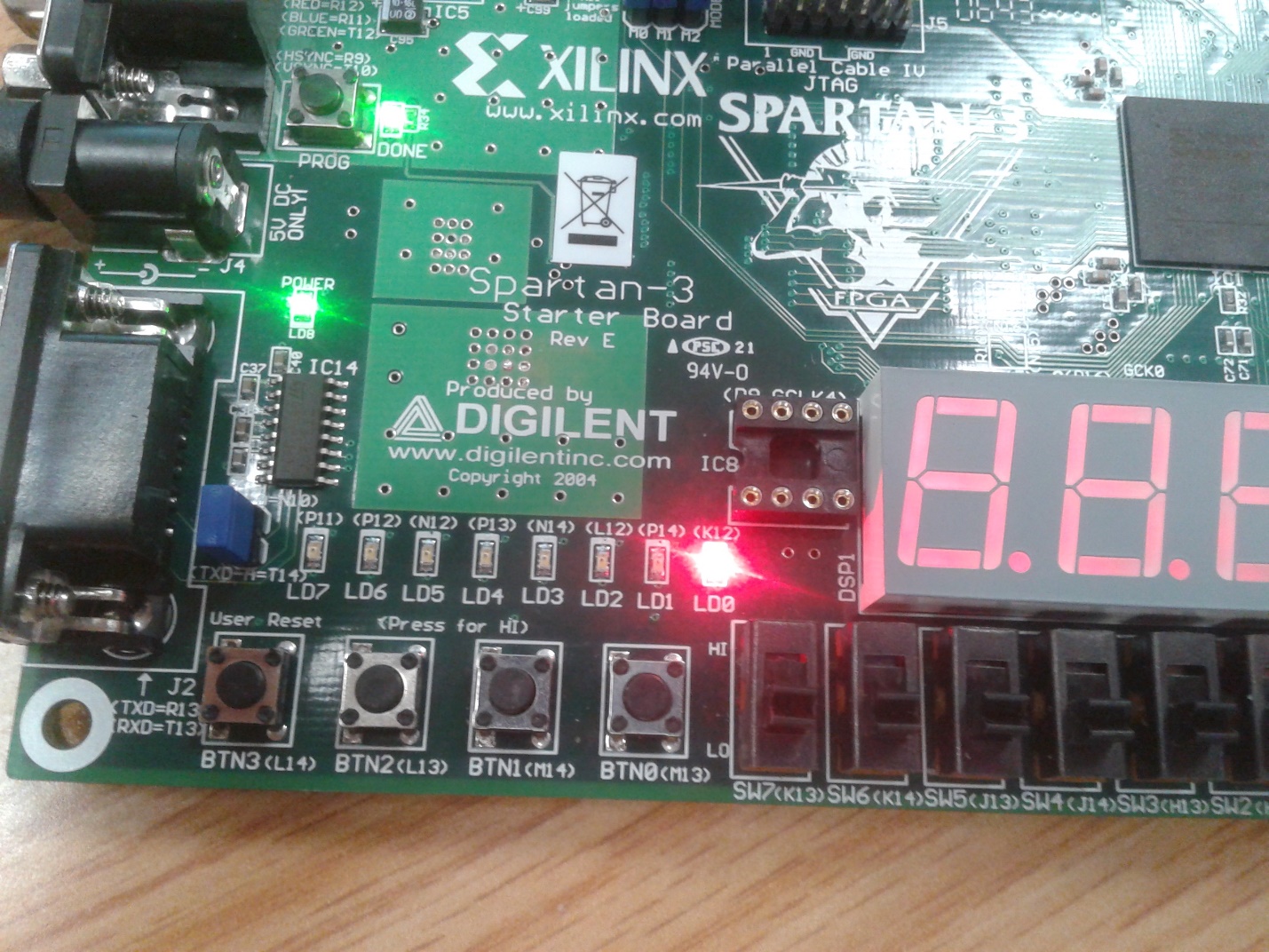


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Submit your Verilog, Picture of FPGA, and UCF file







module top1(clk,reset,Q);

input clk,reset;

output [3:0] Q;

wire clk1;

ClockDivider CD1(clk, reset, clk1);

moore M1(clk1, reset, Q);

endmodule

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module ClockDivider(CLKin,RESET,CLKout);

input CLKin;

input RESET;

output reg CLKout;

parameter CLKoriginal = 50000000;

integer CLKvalue = 0;

always @(posedge CLKin, posedge RESET)

if (RESET == 1'b1)

CLKvalue <= 0;

else

if (CLKvalue == CLKoriginal)

begin

CLKout = 1'b1;

CLKvalue <= 0;

end

else

begin

CLKvalue <= CLKvalue + 1;

CLKout = 1'b0;

end

endmodule

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module moore(clk,rst,W);

input clk, rst;

output [3:0] W;

reg [4:0] state\_reg, state\_next;

parameter S0 = 5'b00001;

parameter S1 = 5'b00010;

parameter S2 = 5'b00100;

parameter S3 = 5'b01000;

parameter S4 = 5'b10100;

parameter S5 = 5'b10010;

always @(posedge clk, posedge rst)

if (rst) state\_reg <= S0;

else

state\_reg <= state\_next;

always @(\*)

case (state\_reg)

S0: state\_next = S1;

S1: state\_next = S2;

S2: state\_next = S3;

S3: state\_next = S4;

S4: state\_next = S5;

S5: state\_next = S0;

default: state\_next = S0;

endcase

assign W = state\_reg[3:0];

endmodule

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# Updated by Wimbo

# Clock

Net "clk" LOC = "T9";

NET "clk" PERIOD = 20ns; # 20ns = 50Mhz

#Net "Socket" LOC = "D9";

#NET "Socket" PERIOD = ??????? ns;

# User Switches

#NET "up" LOC = "F12";

#NET "SW1" LOC = "G12";

#NET "SW2" LOC = "H14";

#NET "SW3" LOC = "H13";

#NET "SW4" LOC = "J14";

#NET "SW5" LOC = "J13";

#NET "SW6" LOC = "K14";

#NET "SW7" LOC = "K13";

# User Buttons

NET "reset" LOC = "M13";

#NET "btn" LOC = "M14";

#NET "BTN2" LOC = "L13";

#NET "BTN3" LOC = "L14";

# LEDs

NET "Q<0>" LOC = "K12";

NET "Q<1>" LOC = "P14";

NET "Q<2>" LOC = "L12";

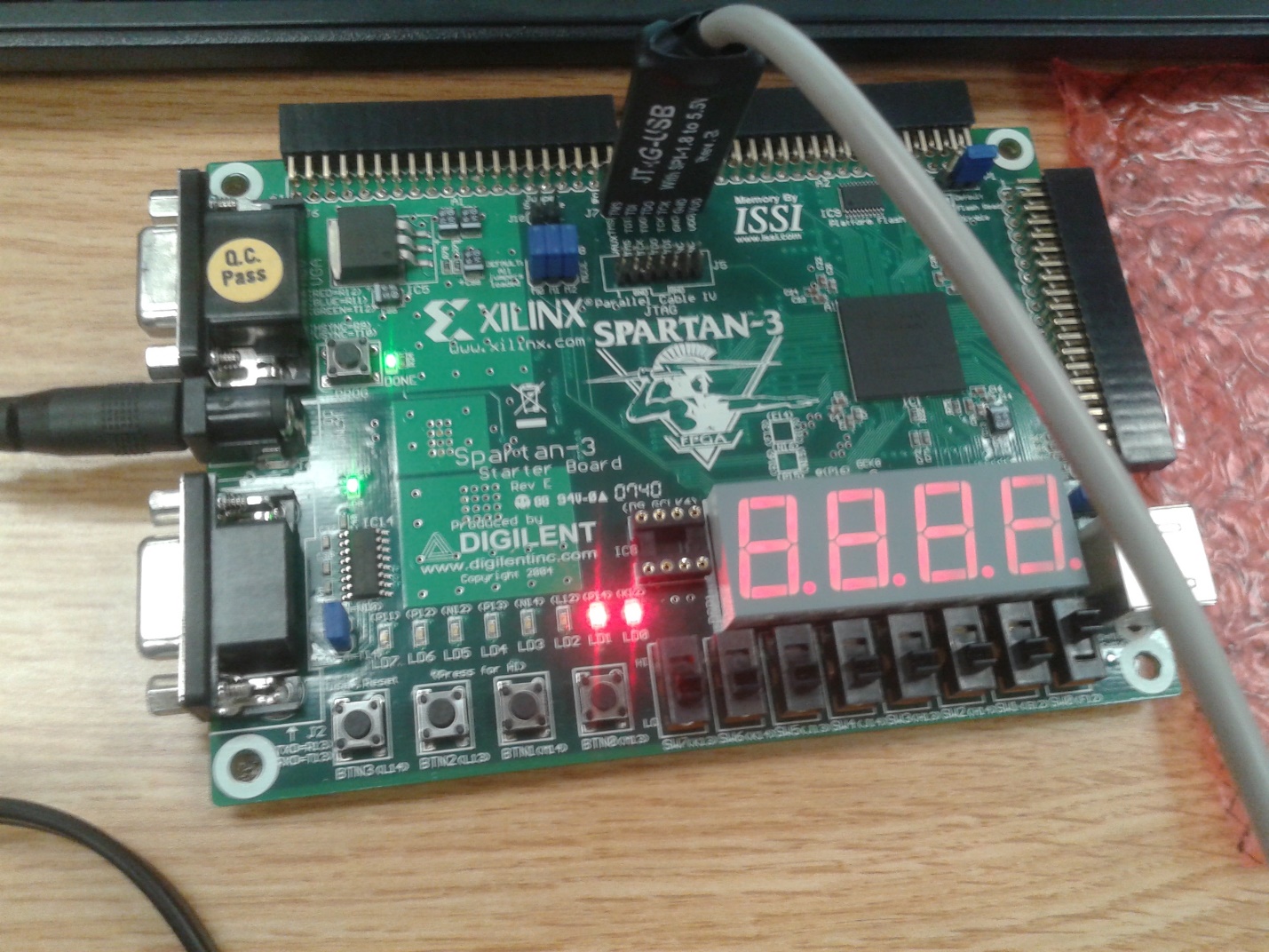
NET "Q<3>" LOC = "N14";

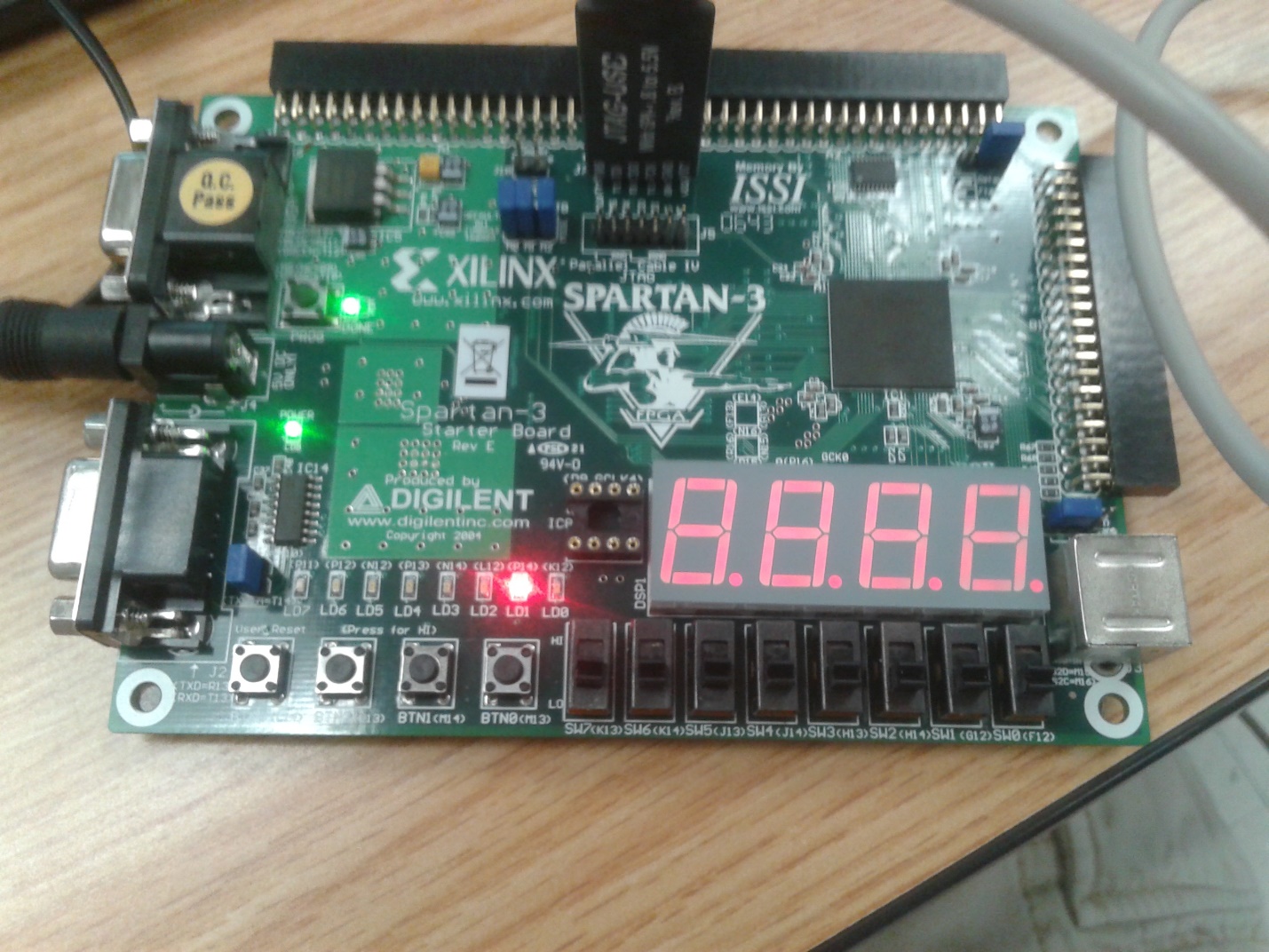
#NET "LD4" LOC = "P13";

#NET "LD5" LOC = "N12";

#NET "LD6" LOC = "P12";

#NET "LD7" LOC = "P11";







module top2(clk,btn,reset,up,Q);

input clk,btn,reset,up;

output [1:0] Q;

wire clk1;

debounce D1(clk,btn,clk1);

mealy M1(clk1, reset, up, Q);

endmodule

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module debounce(clk,btn,btn\_clr);

input clk;

input btn;

output reg btn\_clr;

parameter delay = 650000; //6.5ms delay

integer count=0;

reg xnew=0;

always @(posedge clk)

if (btn != xnew)

begin

xnew <= btn;

count <= 0;

end

else if (count == delay) btn\_clr <= xnew;

else count <= count + 1;

endmodule

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module mealy(clk, rst, up, W);

input clk, rst, up;

output [1:0] W;

reg [1:0] state\_reg, state\_next;

parameter a = 2'b00;

parameter b = 2'b01;

parameter c = 2'b10;

parameter d = 2'b11;

always @(posedge clk, posedge rst)

if (rst) state\_reg <= a;

else

state\_reg <= state\_next;

always @(\*)

case (state\_reg)

a: if(up) state\_next = b;

else state\_next = d;

b: if(up) state\_next = c;

else state\_next = a;

c: if(up) state\_next = d;

else state\_next = b;

d: if(up) state\_next = a;

else state\_next = c;

default: state\_next = a;

endcase

assign W = state\_reg;

endmodule

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# Xilinx Spartan3 Starter Board (Rev E) UCF file

# by Brian Szmyd

# Updated by Wimbo

# Clock

Net "clk" LOC = "T9";

NET "clk" PERIOD = 20ns; # 20ns = 50Mhz

#Net "Socket" LOC = "D9";

#NET "Socket" PERIOD = ??????? ns;

# User Switches

NET "up" LOC = "F12";

#NET "SW1" LOC = "G12";

#NET "SW2" LOC = "H14";

#NET "SW3" LOC = "H13";

#NET "SW4" LOC = "J14";

#NET "SW5" LOC = "J13";

#NET "SW6" LOC = "K14";

#NET "SW7" LOC = "K13";

# User Buttons

NET "reset" LOC = "M13";

NET "btn" LOC = "M14";

#NET "BTN2" LOC = "L13";

#NET "BTN3" LOC = "L14";

# LEDs

NET "Q<0>" LOC = "K12";

NET "Q<1>" LOC = "P14";

#NET "Q<2>" LOC = "L12";

#NET "Q<3>" LOC = "N14";

#NET "LD4" LOC = "P13";

#NET "LD5" LOC = "N12";

#NET "LD6" LOC = "P12";

#NET "LD7" LOC = "P11";